PROCESSOR POWER STATE TRANSITIONS USING SEPARATE LOGIC CONTROL

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ABSTRACT OF THE DISCLOSURE

A computer system having a logic device capable of accepting various chipset controllers and interfacing them with a personal computer processor, the logic device capable of placing the processor into a deep sleep state so that the processor can perform power state transitions. The power state transitions place the processor into a battery optimizing mode or a performance optimizing mode. The logic device allows chipset controllers that may or may not have the capability to perform power state transitions to interface with the processor. The logic device either passes power transition signals through to the processor from the chipset controller or performs the power state transitions. Various chipset and chipset controllers may therefore interface with a processor and are able to switch between battery optimized and performance optimized modes.